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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

TI-38242

Bhupendra Sharma, et al.

Art Unit: 2816

Serial No.: 10/711,532

Examiner:

Filed: September 24, 2004

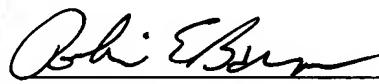
Conf. No: 5531

For: Avoiding Excessive Cross-Terminal Voltages of Low Voltage Transistors Due to
Undesirable Supply-Sequencing in Environments With Higher Supply Voltages

LETTER TO THE OFFICIAL DRAFTSPERSON

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)
I hereby certify that the above correspondence is being
deposited with the U.S. Postal Service as First Class Mail in an
envelope addressed to: Commissioner for Patents, P.O. Box
1450, Alexandria, VA 22313-1450 on January 11, 2005.


Robin E. Barnum

Sir:

Please find enclosed the formal drawings for the subject case. Charge any necessary fees to
Texas Instruments Incorporated, Deposit Account No. 20-0668. **This form is submitted in
triplicate.**

Respectfully submitted,


Abdul Zindani
Attorney for Applicant
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